

5.8GHz Ultra-Low-Power Based Wake-up Receiver for DSRC Application

Myeong Gwan Kim

Department of Electrical and Computer Engineering
Sungkyunkwan University
Suwon, South Korea
alex819@g.skku.edu

Kang Yoon Lee

Department of Electrical and Computer Engineering
Sungkyunkwan University
Suwon, South Korea
klee@skku.edu

Abstract— This paper presents a 5.8GHz Ultra-Low-power based Wake-up Receiver for ETCS (Electronic Toll Collection System) using DSRC (Dedicated Short Range Communication) Transceiver Application. The suggested Wake-up receiver is modulated 5.8 GHz signal and 14 kHz to On-Off Keying (OOK) signal. The Wake-up controller receives a 14 kHz OOK signal and generates WUR_INT signal which goes to MODEM. The suggested Wake-up Receiver (WuRx) is manufactured in 0.13- μ m CMOS bulk of 0.26 mm² technology. When operating at 5.8 GHz frequency, WuRx consumes 3.3 μ W at 0.9V supply and achieves -62dBm sensitivity.

Keywords—WuRx, DSRC, ETCS

I. INTRODUCTION

A circuit for DSRC Application needs to operate with low power consumption. Therefore, the lower the power to operate the WuRx, the better. For this reason, we presents an ultra-low power based WuRx architecture. Section 2 analyzes the proposed architecture by explaining WuRx simply. Section 3 introduces the operating principles through the detailed structure of each block. Section 4 is about Wake-up Controller (WuRC) with RC-oscillator with automatic frequency calibration technique. Section 5 shows the measurement results and simulation results.

II. WAKE-UP RECEIVER ARCHITECTURE

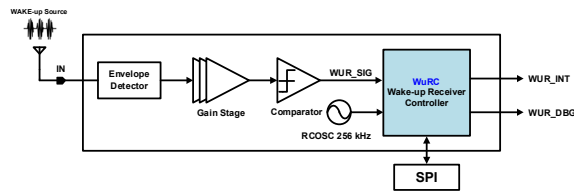


Figure 1. Block Diagram of WuRx

Figure 1. From the viewpoint of the WuRx, detecting and monitoring the input signal frequency for the range of 11kHz to 18kHz. Frequency range and other parameters are configurable for any clock frequency. A signal modulated from a 14 kHz signal to a 5.8 GHz signal enters the WuRx input. It provides envelope output of the input signal when 5.8GHz input enters the envelope detector. The gain stage amplifies the output of

the envelope detector. The amplified signal is compared to the V_{CM} through the comparator and converted into an OOK signal. This signal passing through the WuRx is demodulated by an OOK of 14 kHz. WuRC operates with a 256 kHz clock made by RC-oscillator. WuRC detects and monitors the output signal frequency from the comparator for the range of 11 kHz ~18 kHz. The frequency range and the other parameters are configurable for any clock frequency and generate the Wake-up timer signal.

III. WAKE-UP RECEIVER BUILDING BLOCKS

A. Envelope Detector

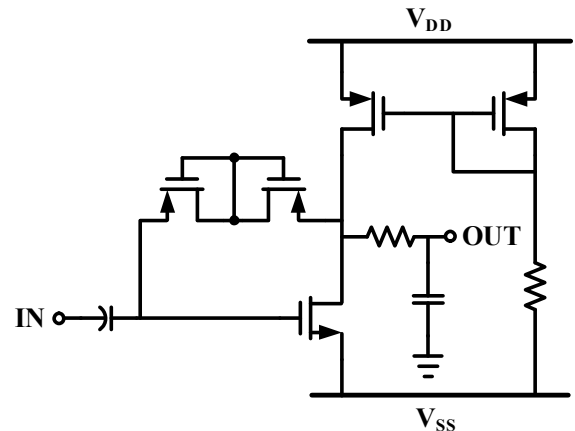


Figure 2. Structure of Envelope Detector

Figure 2 shows a structure of an envelope detector using a common source (CS) amplifier[1]. This structure operates transistors in subthreshold areas. A pseudo-resistor operating as a feedback network is connected to a drain and gate. The output of the CS amplifier is Low Pass Filter (LPF). The envelope detector also detects the peak amplitude of the input signal and scans the envelope line.

B. Gain Stage

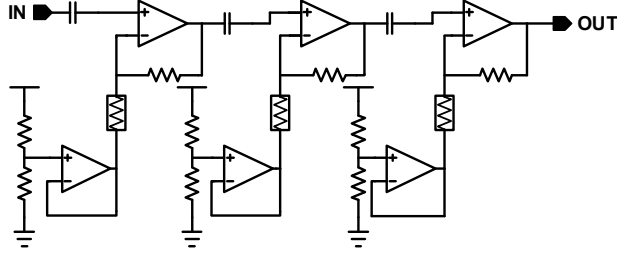


Figure 3. Structure of Gain Stage

This structure consists of a three-stage. Each stage is a negative feedback amplifier. The amplifier is a two-stage amplifier with resistance and compensation capacitors in the gain stage. Each stage has a resistance bank to increase testability during measurement. Each gain step ranges from 30.9 to 34.1 dB, with a total gain of about 100 dB.

C. Comparator

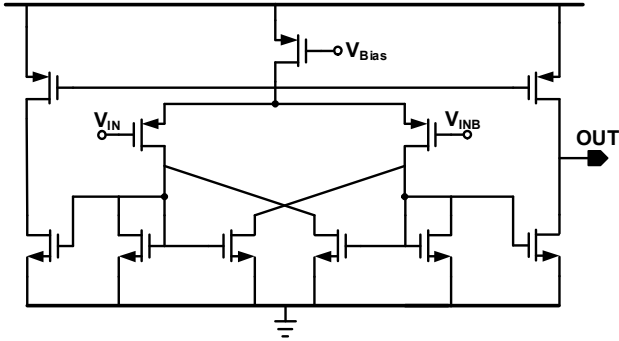


Figure 4. Structure of Comparator

Figure 4. presents a structure of the comparator after the gain stage. It can make a hysteresis by designing a comparator with a latched structure. It needs a hysteresis because of the glitch of the output caused by noise.

IV. WAKE-UP RECEIVER CONTROLLER

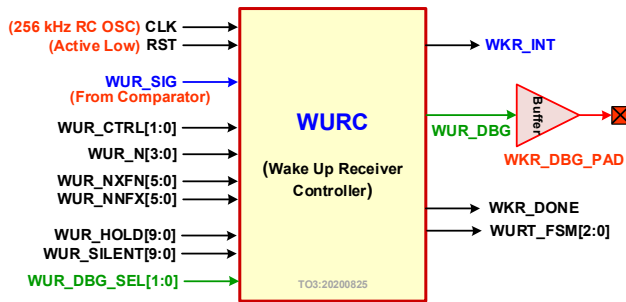


Figure 5. Wake-up Receiver Controller

Figure 5. shows input and output pins of the proposed WuRC. Propose WuRC for incorrect wake-up cases where

noise causes the entire circuit to turn on. WURC operates with 256 kHz RC ring oscillator. 14 kHz Comparator output goes to WUR_SIG path and WURC counts N times of WUR_SIG, and WKR_INT goes high. WUR_N is the input for the number of valid, consecutive WUR_SIG signal cycles before declaring WUR_INT high. WUR_NXFN and WUR_NNFX is change the size of digital filter for the maximum and minimum number for the frequency limit respectively. With WUR_CTRL, the confirmation of the WUR_SIG can be changed. From WUR_DBG output pin, WUR_SIG, input CLK, WUR_INT signals can be measured. All the inputs are controlled by SPI (Serial Peripheral Interface Bus).

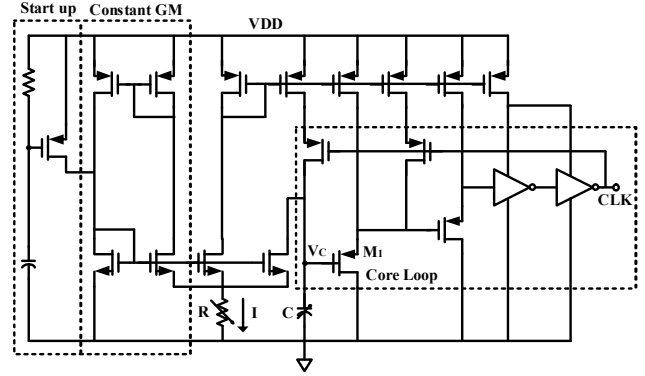


Figure 6. Structure of RC Ring Oscillator

The RC ring oscillator in Figure 6 uses Automatic Frequency Calibration Technology (AFC). AFC receives 4096 times divided XTAL signal, 8 kHz signal as a mask and during that mask time, counts oscillator output and consider if the oscillator output is higher or lower than the exact 256 kHz signal. AFC operates with two options; automatic calibration mode and SPI cap control mode. In automatic calibration mode, the operation is described above. In SPI cap control mode, the cap bank in the oscillator is controlled by SPI.

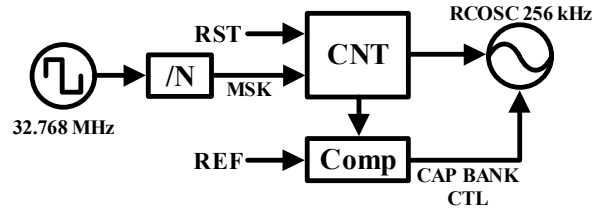


Figure 7. Block Diagram of RC Oscillator Automatic Frequency Calibration

Figure 7. It divides 32.768MHz 4096 times and uses MSK. RCOSC 256 kHz Count at 8 kHz MSK and proceed with CAP Bank Control. It takes 1ms for 8bit CAP Bank Control Calibration.

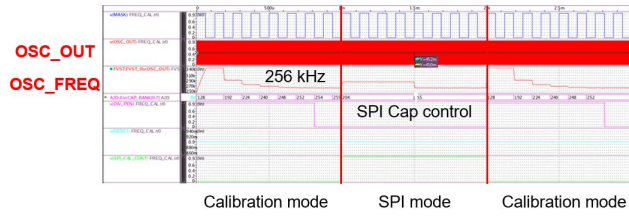


Figure 8. RC-Oscillator Automatic Frequency Calibration Simulation Result

V. EXPERIMENTAL RESULTS

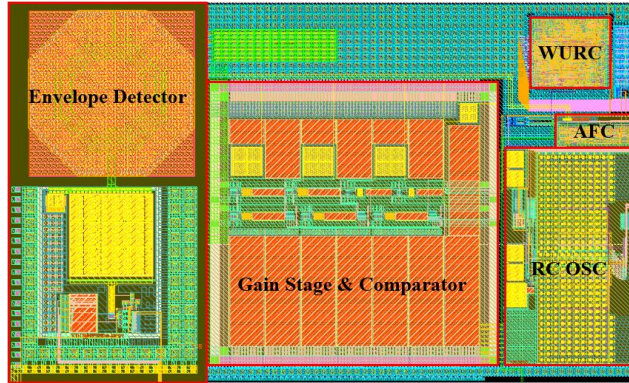


Figure 9. WuRx Layout Photo

The WuRx is manufactured in 0.13 – μm CMOS technology of the top layout as shown in Figure 9. The total active field of the layout is $1004 \mu\text{m} \times 648 \mu\text{m}$.

TABLE I. CURRENT CONSUMPTION

Block	Current Consumption
Envelope Detector	956 nA
Gain Stage	2.3 μA
Comparator	490 nA
WuRC	1.1 μA
RC-oscillator + AFC	1.5 μA
Total	6.346 μA

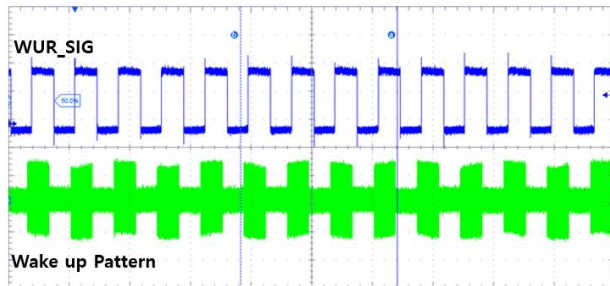


Figure 10. WUR_SIG Measurement Result

Figure 10. is the measurement result of WUR_SIG signal. It is the envelope of the Wake-up pattern, 14 kHz OOK signal.

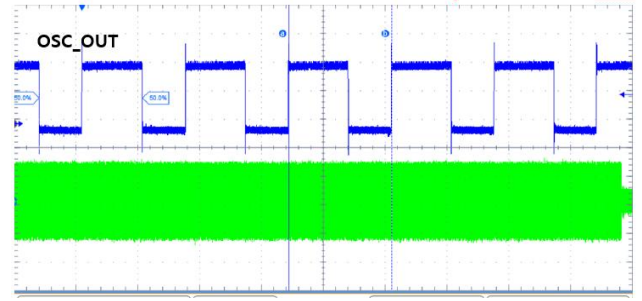


Figure 11. RC-Oscillator Measurement Result

Figure 11. shows the RC ring oscillator output signal. This oscillator output is set by automatic frequency calibration. The output frequency is 257.05 kHz.

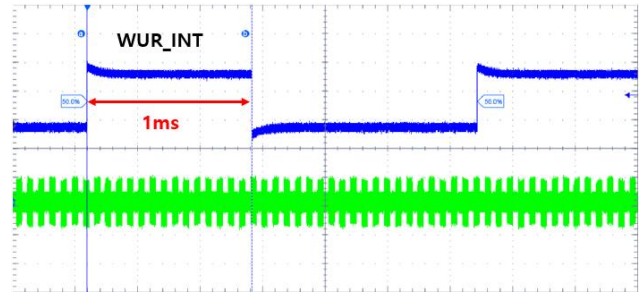


Figure 12. WUR_INT Measurement Result

ACKNOWLEDGMENT

"This work was supported by Institute of Information & communications Technology Planning & Evaluation (IITP) grant funded by the Korea government(MSIT) (No.2020-0-00261, Development of low power/low delay/self-power suppliable RF simultaneous information and power transfer system and stretchable electronic epineurium for wireless nerve bypass implementation)"

REFERENCES

- [1] Yi-bo Su1, Qin Xia1, Li Geng1, and Xin-Ke Liu, "A Highly Linear Low Power Envelope Detector," 2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), 04 July 2019
- [2] Kuang-Wei Cheng, Member, IEEE , Jhih-Syuan Lin, and Shih-En Chen, "Reference-Less Ultra-Low-Power Wake-Up Receiver with Noise Suppression," 2016 URSI Asia-Pacific Radio Science Conference (URSI AP-RASC), 20 October 2016