

# Multi-Switch Integrated Circuit Design for Micro Sensors of Smart Factory

Lee Sung-Hun

dept. ICT Convergence Research  
Gumi Electronics & Information  
Technology Research Institute  
Gumi, South Korea  
leesh@geri.re.kr

Jung Yong-An

dept. ICT Convergence Research  
Gumi Electronics & Information  
Technology Research Institute  
Gumi, South Korea  
yajung@geri.re.kr

Byun Sang-Bong

dept. ICT Convergence Research  
Gumi Electronics & Information  
Technology Research Institute  
Gumi, South Korea  
sbbyun@geri.re.kr

Han Dong-Cheul

dept. ICT Convergence Research  
Gumi Electronics & Information  
Technology Research Institute  
Gumi, South Korea  
cataegu07@geri.re.kr

Cho Soo-Hyun

dept. ICT Convergence Research  
Gumi Electronics & Information  
Technology Research Institute  
Gumi, South Korea  
shcho@geri.re.kr

Kim Seung-Soo

Dept. of SCBU Helic  
Ansys, Inc  
Seoul, South Korea  
seungsso.kim@ansys.com

**Abstract**— In this study, micro multi-switch integrated circuits (IC) for display boards for smart plant sensors were designed and manufactured using a 0.25  $\mu\text{m}$  CMOS process. The switch chip is composed of four single pole single throw (SPST) switches and eight single pole double throw (SPDT) switches, and it was found that the size of the semiconductor IC designed using the simulation with layout effects and a circuit at a transistor level satisfied the target performance even with the process, voltage, and temperature (PVT) variations.

**Keywords**— CMOS, Integrated Circuits, Switch, SPST, SPDT

## I. INTRODUCTION

Due to the recent technological development of the complementary metal oxide semiconductor (CMOS) process, the radio frequency (RF) performance of CMOS is increasingly advancing with the enhancement of a device precision. Despite its shortcomings of CMOS such as leakage current of ultrahigh-frequency caused by high noise resistance and substrate concentrations, the process is widely used in designing wireless transmitter-receiver due to its advantages of low power consumption, high integration, and low production costs in DC status compared to other technologies. As of late, studies on the design of 4 or 8-channel phased-array receiver on a single chip using CMOS process have been conducted [1][2].

Such a multi-channel phased-array receiver or transmitter allows multi-channel on a single chip, significantly reducing the chip area. In this study, the CMOS process was used to develop a single 8-switch-integrated circuit designed to minimize the display board of smart factory sensor data.

## II. CMOS SWITCH IC DESIGN

The display board of smart factory sensor data consists largely of battery, electrophoretic display (EPD), antenna, and various microchips such as bank IC, fingerprint sensor, microprocessor, Bluetooth wireless communication IC, power management (PM) IC, and EPD driver IC. In addition to these chips, eight chips are used, including four load switch chips for power control between the PM IC and various microchips and four analog switch chips for controlling signal flow.

This study designed a combined single IC with eight CMOS switches used for the display cards of smart plant sensor data to minimize the display board size. The reduced board area can boost battery capacity, thus increasing battery life.

### A. Smart plant sensor data display structure study

Major performance indicators to be considered in designing CMOS switch include on-resistance, off-isolation, total harmonic distortion (THD), switching time, and charge injection. These indicators mainly depend on the size of the field-effect transistor (FET) gate. Specifically, as the width of the FET gate used in the CMOS switch increases, the on-resistance shrinks and off-isolation decreases, while THD improves, and switching time and charge injection increase. Some studies reported a method to improve on-resistance such as adding a separate charge pump to boost gate control voltage or adjust body voltage [3][4]. However, these methods require additional circuits, clock, and power consumption. Furthermore, the addition of high resistance to the body has been proposed for performance improvement when the switch operates in the range from less than 10 to dozens of GHz, but it was discovered that the area of additional resistance was considerably large, and the proposed method was not effective in low frequency. A specialized process including BCDMOS should be applied for the applications such as automotive electronics where high electric power is used; however, the target application of this study is smart display requiring low voltage and low current, and thus, a common 0.25  $\mu\text{m}$  CMOS process was used [5][6][7].

### B. Switch IC design for smart plant sensor data display

The simulation was performed to find the input voltage that can achieve lower than the target on-resistance by lowering the voltage from 6 V by 0.1 V while switch control voltage was fixed. 5.5 V was applied to  $V_+$  and switch-on voltage was applied to the logic input since the maximum input voltage in the simulation was 5.5 V.

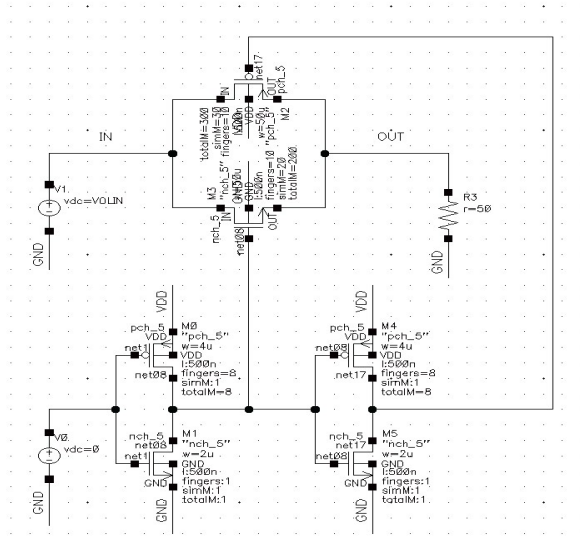


Fig. 2. SPST switch simulation environment (on-resistance)

Figure 2 shows the simulation environment of the SPST switch using Cadence Spectre RF. To improve the reliability of the switch design, PVT variation was taken into account in the simulation. Figure 3 shows the simulation environment of the SPDT switch using Cadence Spectre RF. To improve the reliability of the switch design, PVT variation was taken into consideration in the simulation.

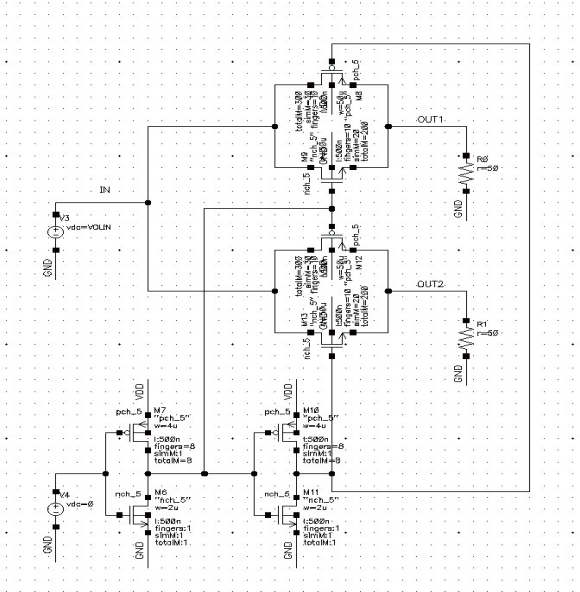


Fig. 3. SPDT switch simulation environment (on-resistance)

### III. RESULT OF SWITCH CHIP DESIGN

Figure 4 demonstrates the simulation results of on-resistance according to three different temperatures at the SS corner of the designed SPST switch. The maximum on-resistance was  $1.1 \Omega$ , and the maximum on-resistance was  $0.85 \Omega$  and  $75 \Omega$ , respectively, at the TT corner and FF corner of the SPST switch. The designed SPST switch showed lower on-resistance than  $1.5 \Omega$ , which is the design target, at nine corners.

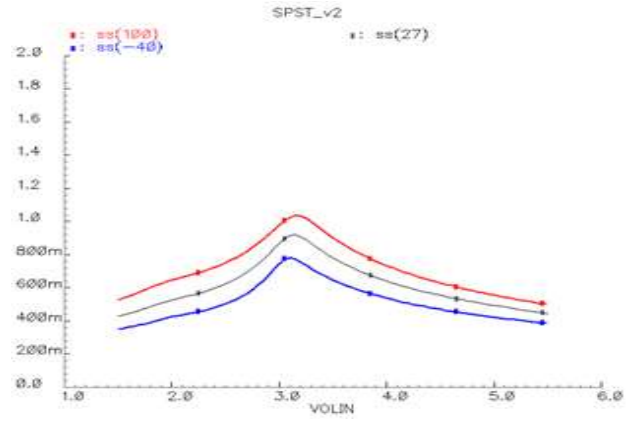


Fig. 4. SS corner simulation result of SPST switch (on-resistance)

Similar to SPST switch design environment, 5.5V was applied to V+ in designing a SPDT switch, as the maximum input voltage was 5.5 V, and switch-on voltage was applied to the logic input. For  $V_{OUT1}$  and  $V_{OUT2}$ , the load resistance was set at  $50 \Omega$  each. The output voltage at  $V_{OUT1}$  and  $V_{OUT2}$  were measured as the switch input voltage was swept from 1.6 V to 5.5V by 0.1V. Using the measured voltage and applied voltage, the on-resistance of the switch can be achieved. Figure 5 demonstrates the simulation results of on-resistance according to three different temperatures at the SS corner of the designed SPDT switch. The maximum on-resistance according to temperature was  $1.05 \Omega$ , and, the maximum on-resistance was  $0.85 \Omega$  and  $0.65 \Omega$ , respectively, at the TT corner and FF corner of the SPDT switch. The designed SPDT switch showed lower on-resistance than  $1.5 \Omega$ , which is the design target, at nine corners.

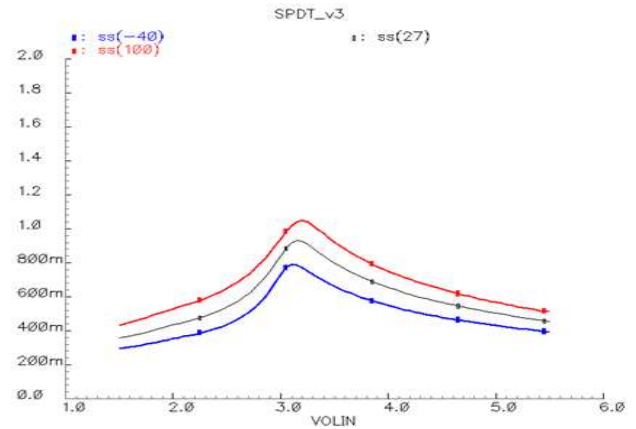


Fig. 5. SS corner simulation result of SPDT switch (on-resistance)

### IV. CONCLUSIONS

In this study, a combined single IC with eight CMOS switches used for the display board of smart plant sensor data was designed. The switch chip consisted of four SPST switches and eight SPDT switches, which was designed to set the switch status by sending independent control signals. The circuit was designed using  $0.25 \mu\text{m}$  CMOS process, and the chip size was  $2.25 \times 2.25 \text{ mm}^2$ . As a result of the simulation, satisfactory performance was achieved in terms of on-resistance and THD. The study found that the area of the

system board can be reduced by more than 10% if the multi-channel switch IC developed is applied to the display board of factory sensors.

#### ACKNOWLEDGMENT

This work was supported by the Institute of Information & Communications Technology Planning & Evaluation (IITP) grant funded by the Korean government (MSIT) (2019-0-00068, Development of Millimeter Wave 5G Components Using Compound Semiconductor Process / 2021-0-00845, 5G·AI-based Textile Factory Creel Process Mobile Manipulator System Development)

#### REFERENCES

- [1] Kwang-Jin Koh, Gabriel M. Rebeiz, "An X- and Ku-Band 8-Element Phased-Array Receiver in 0.18-um SiGe BiCMOS Technology", IEEE Journal of Solid State Circuits, vol. 43, no. 6, Jun. 2008.
- [2] Tiku Yu, Gabriel M. Rebeiz, "A 22--24 GHz 4-Element CMOS Phased Array With On-Chip Coupling Characterization", IEEE Journal of Solid State Circuits, vol. 43, no. 9, Jun. 2008.
- [3] H. Park, "Method for minimizing on-resistance of sampling switch and analog switch circuit", Korea Patent, 10-0757431, Aug. 2007.
- [4] O. Kwon, J. Sul, "CMOS Analog switch circuit", Korea Patent, 10-2013-0079986, Jan. 2015.
- [5] M. C. Yeh, Z. M. Tsai, R. C. Liu, K. Y. Lin, Y. T. Chang, H. Wang, "Design and Analysis for a Miniature CMOS SPDT Switch Using Body-Floating Technique to Improve Power Performance", IEEE Tran. on Microwave Theory and Techniques, vol. 54, no. 1, pp. 31-39, Jan. 2006.
- [6] J. He, "Analysis and Design of 60-GHz SPDT Switch in 130-nm CMOS", IEEE Tran. on Microwave Theory and Techniques, vol. 60, no. 10, pp. 3113-3119, Oct. 2012.
- [7] U. Lee, G. Kwon, H. Lim, H. Shin, "Switch Circuit Design in 0.18  $\mu\text{m}$  BCDMOS for Small Form Factor Automotive Smart Junction Box", Journal of the Institute of Electronics and Information Engineers, vol. 52, no. 3, Mar. 2015.